What is claimed is:

1. An integrated circuit comprising:

a heterojunction thyristor device including an anode terminal, a cathode terminal, a first injector terminal operably coupled to a first quantum well channel disposed between said anode terminal and said cathode terminal, and a second injector terminal operably coupled to a second quantum well channel disposed between said anode terminal and said cathode terminal; and

bias elements that operate said heterojunction thyristor device in a mode that provides substantially linear voltage gain over a range of electrical signals supplied to at least of said first and second injector terminals for output to at least one output node.

2. An integrated circuit according to claim 1, wherein:

said at least one output node comprises said anode terminal.

3. An integrated circuit according to claim 1, wherein:

said at least one output node comprises said cathode terminal.

4. An integrated circuit according to claim 1, wherein:

open loop voltage gain provided by said heterojunction thyristor device is at least 200.

5. An integrated circuit according to claim 4, wherein:

said open loop voltage gain is greater than 50,000.

6. An integrated circuit according to claim 1, wherein:

said bias elements include at least one current source that supplies a DC current to at least one of said first and second injector terminals, said DC current controlling the amount of voltage gain provided by said heterojunction thyristor device.

7. An integrated circuit according to claim 6, wherein:

said first quantum well channel comprises an n-type modulation doped quantum well structure and said second quantum well channel comprises a p-type modulation doped quantum well structure; and

said bias elements include a first DC current source operably coupled to said n-type modulation doped quantum well structures and a second DC current source operably coupled to said p-type modulation doped quantum well structure.

8. An integrated circuit according to claim 7, wherein:

said bias elements include a first bias resistor operably coupled between a high voltage supply and said anode terminal and a second bias resistor operably coupled between said cathode terminal and a low voltage supply.

9. An integrated circuit according to claim 1, wherein:

said bias elements provide a current passing from said anode terminal to said cathode terminal that is below a characteristic hold current for said heterojunction thyristor device to thereby inhibit switching of said heterojunction thyristor device.

10. An integrated circuit according to claim 1, further comprising:

a first coupling capacitor operably coupled to said first injector terminal, and a second coupling capacitor operably coupled to said second injector terminal.

11. An integrated circuit according to claim 1, wherein:

a differential input signal is supplied to said first and second injector terminals.

12. An integrated circuit according to claim 11, wherein:

said at least one output node comprises said cathode terminal which produces a single-ended output signal that represents said differential input signal amplified by a large inverted characteristic voltage gain.

13. An integrated circuit according to claim 11, wherein:

said at least one output node comprises said anode terminal which produces a single-ended output signal that represents said differential input signal amplified by a large non-inverted characteristic voltage gain.

14. An integrated circuit according to claim 11, wherein:

said at least one output node comprises said cathode terminal and said anode terminal which together produce a differential output signal that represents said differential input signal amplified by a large characteristic voltage gain.

15. An integrated circuit according to claim 1, further comprising:

an output buffer stage coupled to at least one of said anode terminal and said cathode terminal of said heterojunction thyristor device.

16. An integrated circuit according to claim 1, wherein:

said heterojunction thyristor device is formed from a multilayer structure of group III-V materials.

17. An integrated circuit according to claim 1, wherein:

said heterojunction thyristor device is formed from a multilayer structure of strained silicon materials.

18. An integrated circuit according to claim 1, wherein:

said heterojunction thyristor device further comprises a p-channel FET transistor formed on said substrate and an n-channel FET transistor formed atop said p-channel FET transistor.

19. An integrated circuit according to claim 18, wherein:

said p-channel FET transistor comprises a modulation doped p-type quantum well structure, and wherein said n-channel FET transistor comprises a modulation doped n-type quantum well structure.

20. An integrated circuit according to claim 19, wherein:

said p-channel FET transistor includes a bottom active layer,

said n-channel FET transistor includes a top active layer, and

said heterojunction thyristor device further comprises an anode terminal operably coupled to said top active layer, a cathode terminal operably coupled to said bottom active layer, and an injector terminal operably coupled to at least one of said modulation doped n-type quantum well structure and said modulation doped p-type quantum well structure.

21. An integrated circuit according to claim 20, wherein:

said heterojunction thyristor device further comprises an ohmic contact layer, a metal layer for said anode terminal that is formed on said ohmic contact layer, and a plurality of p-type layers formed between said ohmic contact layer and said n-type modulation doped quantum well structure.

22. An integrated circuit according to claim 21, wherein:

said plurality of p-type layers are separated from said n-type modulation doped quantum well structure by undoped spacer material.

23. An integrated circuit according to claim 21, wherein:

said plurality of p-type layers include a top sheet and bottom sheet of planar doping of highly doped p-material separated by a lightly doped layer of p-material, whereby said top sheet achieves low gate contact resistance and said bottom sheet defines the capacitance of said n-channel FET transistor.